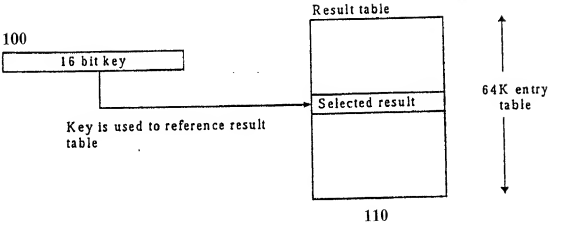


FIG. 1

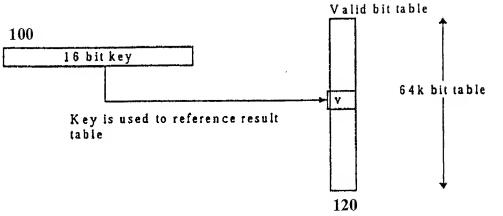


FIG. 2

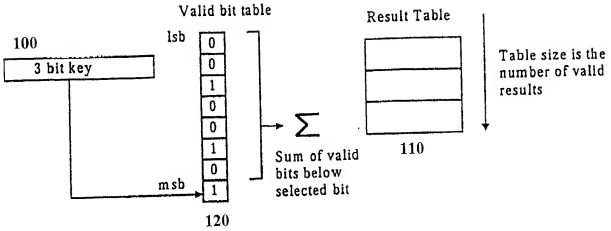


FIG. 3

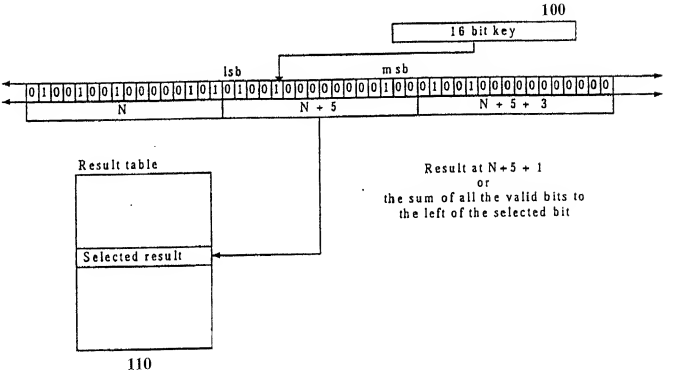


FIG. 4

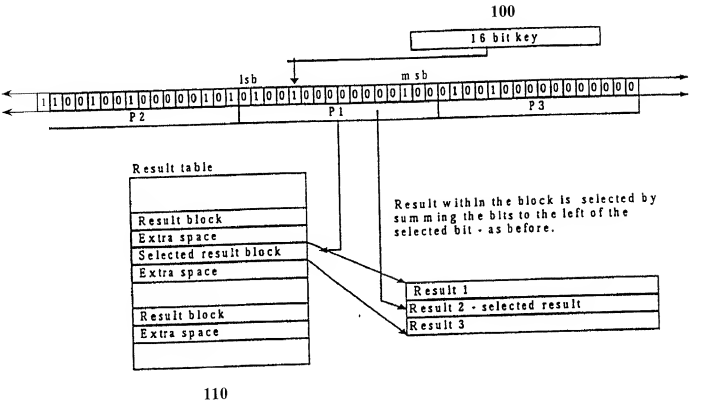

100
16 bit key
lsb
msb
P2
P1
P3
Result table
Result block
Extra space
Selected result block
Extra space
Result block
Extra space
Result within the block is selected by summing the bits to the left of the selected bit - as before.
Result 1
Result 2 - selected result
Result 3
110

FIG. 5

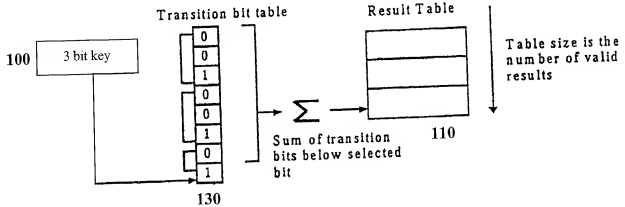

Transition bit table
Result Table
100
3 bit key
0
0
1
0
0
1
0
1
Σ
Sum of transition bits below selected bit
110
Table size is the number of valid results
130

FIG. 6

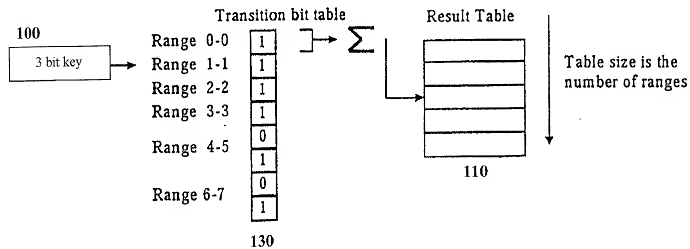

100
3 bit key
Transition bit table
Range 0-0
Range 1-1
Range 2-2
Range 3-3
Range 4-5
Range 6-7
1
1
1
1
0
1
0
1
130
Σ
Result Table
110
Table size is the
number of ranges

FIG. 7

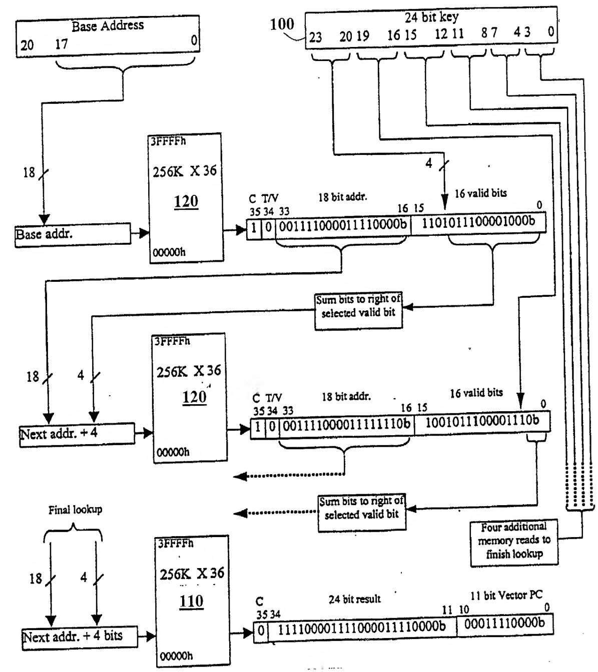

Base Address
20 17 0
100
24 bit key
23 20 19 16 15 12 11 8 7 4 3 0
18
4
Base addr.
3FFFFh
256K X 36
120
00000h
C T/V
35 34 33
18 bit addr.
16 15
16 valid bits
0
1 0 001111000011110000b 1101011100001000b
Sum bits to right of selected valid bit
18
4
Next addr. + 4
3FFFFh
256K X 36
120
00000h
C T/V
35 34 33
18 bit addr.
16 15
16 valid bits
0
1 0 001111000011111110b 1001011100001110b
Sum bits to right of selected valid bit
Four additional memory reads to finish lookup
Final lookup
18
4
Next addr. + 4 bits
3FFFFh
256K X 36
110
00000h
C
35 34
24 bit result
11 10
11 bit Vector PC
0
0 111100001111000011110000b 00011110000b

FIG. 8

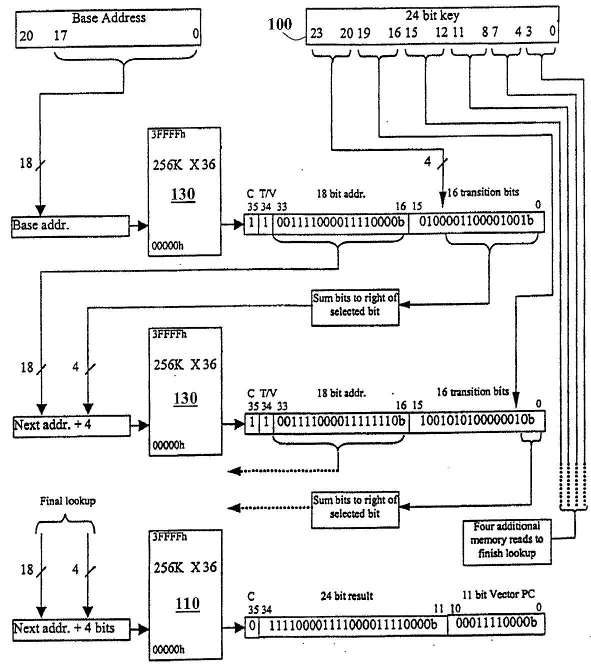

Base Address
20 17 0
24 bit key
23 20 19 16 15 12 11 8 7 4 3 0
100
18
4
Base addr.
3FFFFh
256K X 36
130
00000h
C T/V
35 34 33
18 bit addr.
16 15
16 transition bits
0
1 1 001111000011110000b 0100001100001001b
Sum bits to right of selected bit
18
4
Next addr. + 4
3FFFFh
256K X 36
130
00000h
C T/V
35 34 33
18 bit addr.
16 15
16 transition bits
0
1 1 001111000011111110b 1001010100000010b
Sum bits to right of selected bit
Four additional memory reads to finish lookup
Final lookup
18
4
Next addr. + 4 bits
3FFFFh
256K X 36
110
00000h
C
35 34
24 bit result
11 10
11 bit Vector PC
0
0 111100001111000011110000b 00011110000b

FIG. 9

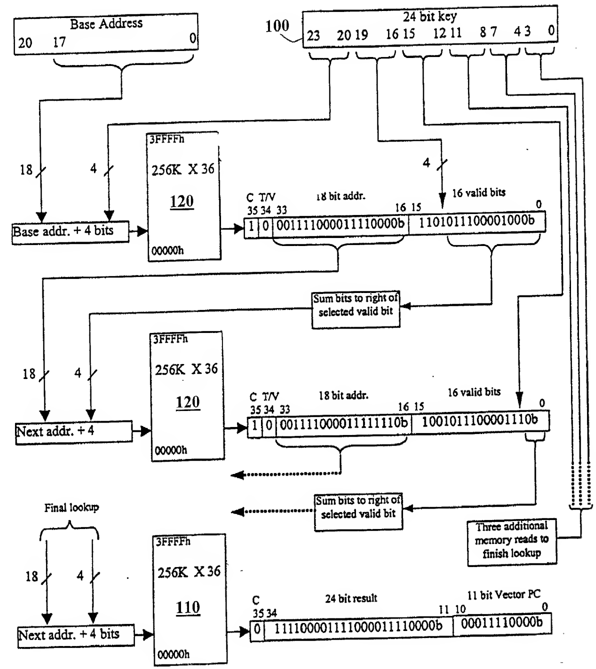

Base Address
20 17 0
24 bit key
23 20 19 16 15 12 11 8 7 4 3 0
100
18
4
3FFFFh
256K X 36
120
00000h
Base addr. + 4 bits
C T/V
35 34 33
18 bit addr.
16 15
16 valid bits
0
1 0 001111000011110000b 1101011100001000b
Sum bits to right of selected valid bit
Next addr. + 4
1 0 001111000011111110b 1001011100001110b
Three additional memory reads to finish lookup
Final lookup
Next addr. + 4 bits
110
C
35 34
24 bit result
11 10
11 bit Vector PC
0 111100001111000011110000b 00011110000b

FIG. 10

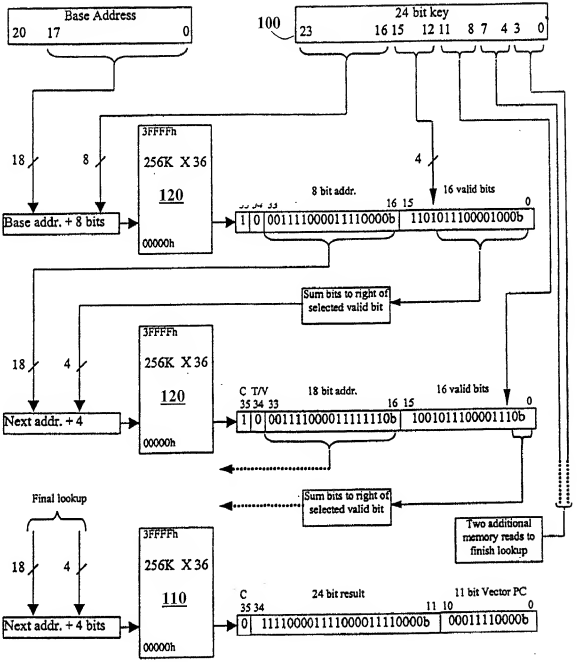


FIG. 11

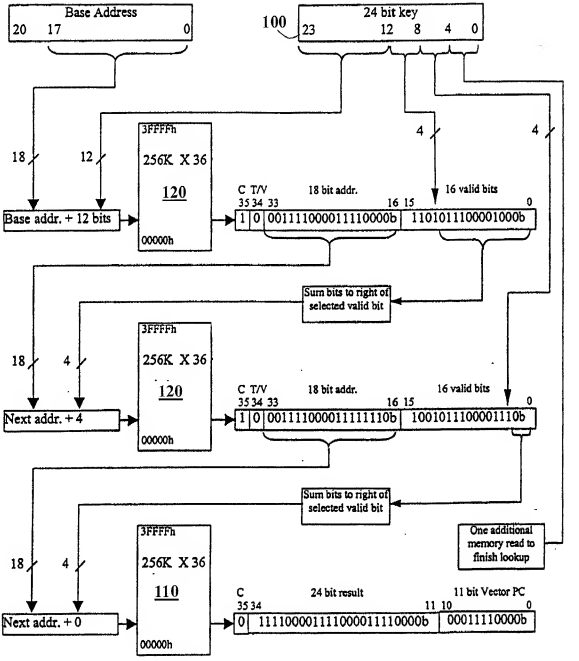


FIG. 12

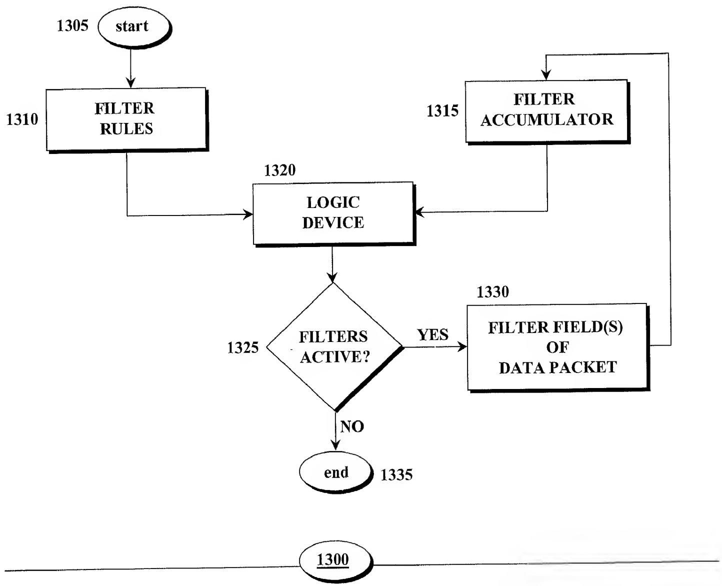

1305
start
1310
FILTER
RULES
1315
FILTER
ACCUMULATOR
1320
LOGIC
DEVICE
1325
FILTERS
ACTIVE?
YES
1330
FILTER FIELD(S)
OF
DATA PACKET
NO
end
1335
1300

FIG. 13

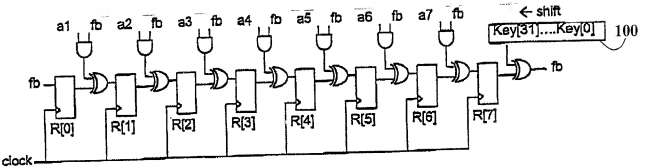
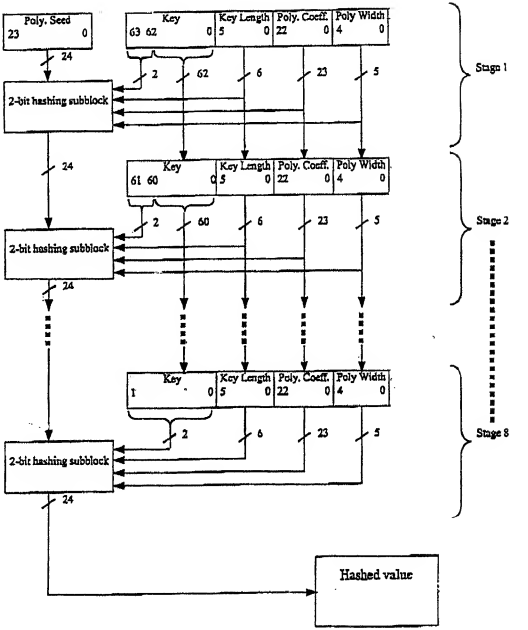

a1
fb
a2
fb
a3
fb
a4
fb
a5
fb
a6
fb
a7
fb
← shift
Key[31]....Key[0]
100
fb
fb
R[0]
R[1]
R[2]
R[3]
R[4]
R[5]
R[6]
R[7]
clock

FIG. 14

FIG. 15



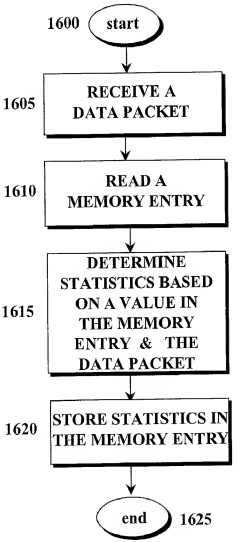


FIG. 16